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A Standard Microsyste ompany

CG 5004L-1

Preliminary Specifications

Dot Matrix Character Generator

128 Characters of 7 × 11 Bits

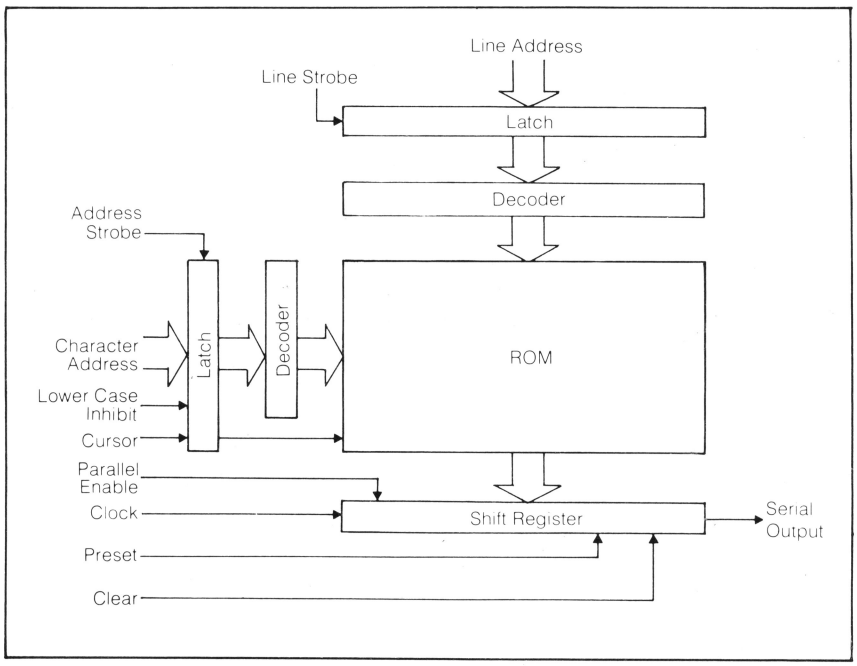
General Description

The SMC CG5004L is a high speed character generator designed to display 128 characters in a 7X11 dot matrix. It is fabricated using SMC's MOS N channel Silicon Gate COPLAMOS® Process which provides a higher functional density and speed on a monolithic chip than conventional MOS technology. The CG5004L is designed for use in row raster scan CRT displays, printer character generators, panel displays, billboards, light emitting diodes and other character generator displays.

The CG5004L-1 contains the complete 128 ASCII encoded character set and uses the full 7X11 dot matrix capability, producing a character having extremely high quality, high resolution and definition.

Features

- MOS N channel Silicon Gate COPLAMOS® Process
- On-Chip parallel to serial shift register
- Directly TTL compatible on all Inputs/Outputs
- ASCII encoded
- 128 Characters — full ASCII set
- 7X11 dot matrix
- No descender circuitry required
- Buffered line address
- Buffered character address
- Static Operation
- Power consumption<400 mw
- +5 volt operation
- Lower case inhibit
- Cursor control
- Hermetic ceramic 24 pin DIP package
- Input protected



Pin Functions

Pin No. 1
V_{BB} Power Supply

This pin should be wired to the cathode of a diode, with the anode connected to ground. Under these conditions, the circuit's substrate (or body) is pumped a few tenths of a volt negative by the on-chip voltage generator.

Pin No. 2
SO Serial Output

The output of the shift register is clocked out on this pin. The serial input to this shift register is internally grounded; thus zeroes are shifted in while data is shifted out.

Pin No. 3
V_{DD} Power Supply

+5 volts.

Pin No. 4
LS Line Strobe

A positive pulse on this input enters data from the L_1, L_2, L_4, L_8 lines into the line address holding register. The LS input may be left open, in which case it is pulled up to V_{DD} by an internal resistor. Data on the L_1 to L_8 inputs is then entered directly into the register without any latching action.

Pin No. 5
PRST Preset

A high level on this input forces the last stage of the shift register and the serial output to a high level.

Pins Nos. 6, 8, 9, 10
L_1, L_2, L_4, L_8 Line Address

A binary number, N, on these four inputs addresses the Nth line of the character font for N = 1 —11. If lines 0, 12, 13, 14 or 15 are addressed the parallel inputs to the shift register are all forced low.

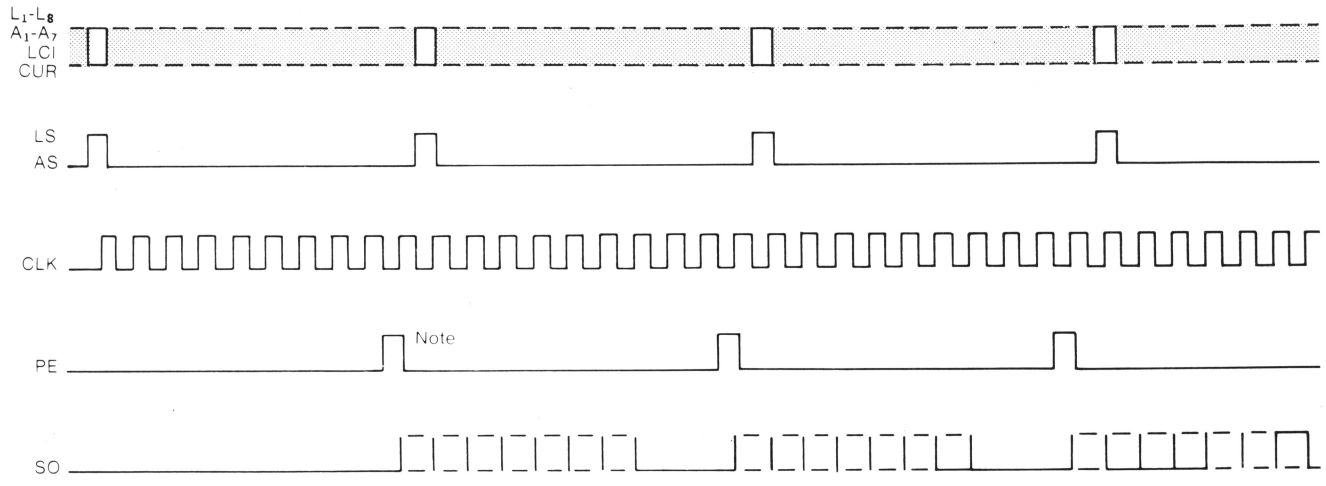
Pin No. 7
CLR Clear

A high level on this input forces the last stage of the shift register and the serial output to a low level. If both the Preset and Clear inputs are brought high simultaneously, the Serial Output is disabled and may be wire-ORed.

Pin Nos. 11-17
A_1-A_7 Character Address

The seven-bit word on these inputs is decoded internally to address one of the 128 available characters.

Typical System Timing



Note The PE input over-rides the serial inputs to the shift-register stages and is independent of the CLK level. However, to avoid timing uncertainties, it is recommended that PE only be brought low after the serial inputs are disabled, i.e. after the CLK has gone to a high level.

Pin No. 18
LCI Lower Case Inhibit

A high level on this input transforms the address of a lower case character into that of the equivalent upper case character. This is achieved by forcing A6 low whenever A7 and LCI are high.

Pin No. 19
AS Address Strobe

A positive pulse on this input enters data from the A1-A7, LCI and CUR inputs into the holding register. The AS input may be left open, in which case it is pulled up to VDD by an internal resistor. The data on the A1-A7, LCI and Cursor inputs is then entered directly into the register without any latching action.

Pin No. 20
CUR Cursor

A high level on this input causes the cursor pattern to be superimposed on the pattern of the character addressed, i.e., the two patterns are OR-ed to generate the parallel inputs to the shift register. The cursor is presented as a double underscore on rows 10 and 11.

Pin No. 21
CLK Clock

A high level on this input transfers data from the shift register to the Serial Output. Data is shifted into each stage of the register while the CLK input is low.

Pin No. 22
VGG Power Supply

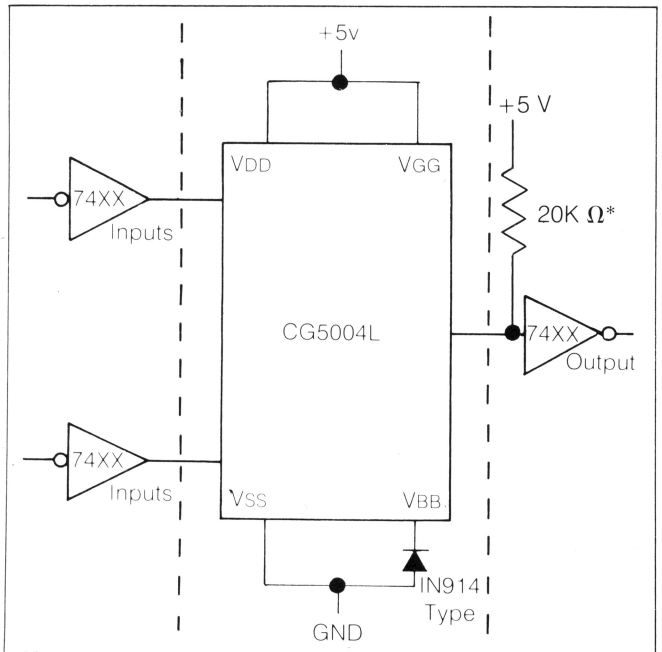
+ 5 volts.

Pin No. 23
PE Parallel Enable

A high level on this input loads the word at the output of the ROM into the shift register. The PE input must then be brought low again to allow the shift register to clock out this word.

Pin No. 24
VSS Power Supply

Ground.



*for additional high level noise immunity.

Test Conditions

Electrical Characteristics

	Nanoseconds		
	Min	Typ	Max
Pulse Width			
Clock, high	50	25	
Clock, low	150	100	
Address Strobe, high	300		
Line Strobe, high	300		
Parallel Enable, high	50		
Preset, high	50		
Clear, high	50		
Access Time		750	1000
Propagation Delay			
clock to serial output		100	160

A1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
A2	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
A3	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
A4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
A7A6A5																
000																
001																
010																
011																
100																
101																
110																
111